Low $D_{it}$, Thermodynamically Stable Ga$_2$O$_3$–GaAs Interfaces: Fabrication, Characterization, and Modeling

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Abstract—Thermodynamically stable, low $D_{it}$, amorphous Ga$_2$O$_3$-(100) GaAs interfaces have been fabricated by extending molecular beam epitaxy (MBE) related techniques. We have investigated both in situ and ex situ Ga$_2$O$_3$ deposition schemes utilizing molecular beams of gallium oxide. The in situ technique employs Ga$_2$O$_3$ deposition on freshly grown, atomically ordered (100) GaAs epitaxial films in ultrahigh vacuum (UHV); the ex situ approach is based on thermal desorption of native GaAs oxides in UHV prior to Ga$_2$O$_3$ deposition. Unique electronic interface properties have been demonstrated for in situ fabricated Ga$_2$O$_3$–GaAs interfaces including a midgap interface state density $D_{it}$ in the low $10^{10}$ cm$^{-2}$ eV$^{-1}$ range and an interface recombination velocity $S$ of 4000 cm/s. The existence of strong inversion in both n- and p-type GaAs has been clearly established. We will also discuss the excellent thermodynamic and photochemical interface stability. Ex situ fabricated Ga$_2$O$_3$–GaAs interfaces are inferior but still of a high quality with $S = 9000$ cm/s and a corresponding $D_{it}$ in the upper $10^{10}$ cm$^{-2}$ eV$^{-1}$ range.

We also developed a new numerical heterostructure model for the evaluation of capacitance-voltage (C-V), conductance-voltage (G-V), and photoluminescence (PL) data. The model involves selfconsistent interface analysis of electrical and optoelectronic measurement data and is tailored to the specifics of GaAs such as band-to-band luminescence and long minority carrier response time $\tau_F$. We will further discuss equivalent circuits in strong inversion considering minority carrier generation using low-intensity light illumination.

1. INTRODUCTION

LOW-POWER technologies are key to the widespread use of high-performance portable systems such as portable computers, cellular telephones, personal communicators, PDAs, medical devices, etc. At the present time, bulk Si CMOS offers significant advantages in terms of integration level and cost; however, reductions in circuit speed of bulk Si CMOS are anticipated as the power supply is scaled to 1 V or below [1], [2]. The decrease in circuit speed can be compensated only to a certain extent by innovative technologies (e.g., silicon on insulator [3]) and parallel architectures or pipelining (e.g., [4]). Consequently, the natural choice for low-power, high-speed/frequency devices remain technologies using high-mobility materials such as GaAs and related compounds (e.g., [5], [6]). Complementary GaAs technologies exhibit advantages over bulk Si such as low parasitic capacitance and process simplicity similar to SOI. Beyond the improvements provided by SOI, high-mobility technologies also offer very low "on" voltage and high transconductance at low voltage resulting in optimum speed/power performance at supply voltages of 1 V and below. At low supply voltages, complementary GaAs technologies have demonstrated a 4–9 times lower power consumption with the same gate delay when compared to SOI [5]. Further, high transconductance is essential for minimizing interconnect delay [7]. One of the key remaining issues for GaAs, however, is the lack of insulating layers providing low $D_{it}$ and stable device operation. The use of MODFET's in present complementary GaAs technologies causes excessive gate leakage currents and results in unacceptable high stand-by power for portable systems. Gate leakage also affects the gain and limits the maximum output power in power amplifiers using a single power supply.

This paper presents an approach to overcome the above described bottleneck of insulating layers on GaAs providing low $D_{it}$ and stable device operation. We will illustrate how the extension of MBE toward deposition of gallium oxide molecules has provided the required ingredients for the implementation of thermodynamically stable, low $D_{it}$ oxide-GaAs interfaces. Pivotal aspects include an extremely low GaAs surface exposure to impurities (<10–100 Langmuirs, $1L = 10^{-6}$ torr s) and the preservation of GaAs bulk and surface stoichiometry [8], the complete exclusion of GaAs surface oxidation [9]–[11], and the requirement of a specific atomic structure associated with the interfacial atoms of GaAs and the deposited molecules [12]. We will emphasize that these requirements are met when specific molecules are deposited in situ under ultrahigh vacuum conditions. Further, we will discuss first results obtained using an ex situ deposition scheme which is applicable to GaAs surfaces exposed to room air and/or processing environments during fabrication of devices.

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The following sections will cover in situ and ex situ wafer fabrication, interface characterization, and modeling.

II. WAFER FABRICATION

The 2-in wafers were fabricated using a multiple-chamber UHV system [13]. The wafer fabrication was comprised of 1.5-µm thick n-type (1.6 x 10^16 cm^-3) or p-type (4.4 x 10^16 cm^-3) GaAs epilayers grown by solid source MBE on heavily Si or Zn-doped (100) GaAs substrates, respectively. After completion of GaAs growth, in situ and ex situ schemes were investigated as described in the following paragraphs.

A. In Situ Deposition

After completion of GaAs growth, the freshly grown film with an As-stabilized (2 x 4) surface was transferred under a vacuum of 6 x 10^-11 Torr to another chamber (background pressure = 10^-10 Torr) for oxide deposition. Fig. 1 shows the pressure (solid line) and the corresponding GaAs surface exposure (dashed line) which is typically observed prior to opening the shutter for oxide deposition. The time t_c and t_s is the time of completion of GaAs growth and the time at which the shutter was opened for oxide deposition, respectively. The GaAs surface was exposed to a pressure not higher than 10^-10 Torr during the transfer and heating of the substrate to the deposition temperature T_s. For the last 2 min, the e-beam was turned on to heat up the oxide target. Only then did the GaAs surface begin to experience the pressure from 10^-10 to 10^-7 Torr. The pressure rise (predominantly oxygen) was caused by vaporization and thermal dissociation of the oxide targets during e-beam heating. Note that the typical GaAs surface exposure prior to opening the shutter for oxide deposition (t_c < t < t_s) was ≤10 Langmuirs. Based on typical initial sticking coefficients for oxygen (e.g., [14]), the GaAs surface impurity coverage is estimated at 10^-5-10^-3% of a mono-layer or 10^9-10^10 surface impurities/cm^2 prior to deposition.

The preservation of surface periodicity and atomic order was investigated by in situ reflection high-energy electron diffraction (RHEED) in the time interval t_c < t < t_s. RHEED pictures acquired from a (100) GaAs surface at the time t_c and t_s (T_s = 360 °C) are identical, showing a (2 x 4) reconstructed, As-stabilized surface (Fig. 2). The surface reconstruction (2 x 4) and long streaky RHEED patterns indicate an atomically ordered and contamination free surface. Consequently, the surface atomic order and periodicity is not affected by exposure to impurity gases of less than 10 Langmuirs in our experiments and the surface stoichiometry is completely preserved prior to opening the shutter for oxide deposition at time t_s.

B. Ex Situ Deposition

Here, the wafers were removed from the MBE chamber after completion of GaAs growth, exposed to room air for at least three days, and then loaded into the oxide deposition chamber (background pressure = 10^-10 Torr). The native oxides which built up on the GaAs surface during air exposure were thermally desorbed without As overpressure at a substrate temperature T_s of 580-600 °C. RHEED was used to monitor the process of native oxide desorption. No surface reconstruction was observed and the RHEED streaks were not continuous [15]. The latter is indicative of surface roughness and residual contamination.

Finally, oxide films were deposited at substrate temperatures T_s ranging from room temperature to ≈ 600 °C using molecular beams of gallium oxide. Single crystal Gd_2Ga_2O_12 [16] was used as a source material and evaporated by an e-beam technique. The use of Gd_2Ga_2O_12 was motivated by the unavailability of single crystal Ga_2O_3 and had led to the first successful deposition of gallium oxide molecules forming very uniform Ga_2O_3 films on GaAs [17]. Note that Ga_2O_3 exhibits a high sublimation temperature of 1725 °C [18]. The fabrication of MOS capacitors was completed by deposition of Ti/Au metal dots using a standard shadow mask process.

Reference wafers with identical GaAs epitaxial structure and substrate were also fabricated in the same solid-source III-V chamber using 1) no oxide deposition (bare samples), and 2) Al_{0.45}Ga_{0.55}As interfaces.

III. STRUCTURAL PROPERTIES

The chemical composition of Ga_2O_3–GaAs interfaces has been investigated by X-ray photoelectron spectroscopy (XPS). Compositional profiles and the crystallographic structure of the deposited oxide films have been studied by Rutherford backscattering spectrometry (RBS), secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM), and RHEED, respectively.

Fig. 3 shows measured (solid line) and simulated (dashed line) RBS spectra of a gallium oxide film deposited in situ on GaAs at T_s = 360 °C. The ratio of Ga with oxygen was determined to 43:55.5. Previously published results indicated...
that the nonstoichiometry of the Ga$_2$O$_3$ film is due to incorporation of excess elemental Ga [17]. Further, Ga$_2$O$_3$ films using e-beam evaporation of Gd$_2$Ga$_2$O$_{12}$ typically exhibit a nonuniform Gd distribution characterized by a virtually Gd free interfacial region and a peak in Gd concentration at the film surface (see Fig. 3). Our characterization methods (including XPS and SIMS) can not completely exclude the presence of Gd at the interface and possible effects of Gd on electronic interface properties are not known at this time. The presence of Gd in the bulk oxide film may affect electrical measurements conducted on MOS structures to be discussed later. In the following, we will refer to the oxide films as Ga$_2$O$_3$ films. Fig. 4 shows the plan view TEM micrograph and the corresponding electron diffraction pattern of a Ga$_2$O$_3$ film deposited \textit{in situ} on GaAs at $T_s = 360 ^\circ$C. As observed from TEM (and RHEED) studies, Ga$_2$O$_3$ films are amorphous with partial ordering in a completely disordered state for increased deposition temperature [17], [19]. The amorphous phase of Ga$_2$O$_3$ films eludes problems arising from lattice-mismatched interfaces.

Interfacial As 3d core level spectra were acquired using a Perkin Elmer 5600 series XPS spectrometer equipped with a monochromatic Al K\textalpha{} X-ray source. The photon energy was 1486.6 eV. Depth profiling was done \textit{in situ} in a UHV chamber (background pressure $= 5 \times 10^{-10}$ torr) by Ar sputtering using an ion gun at 4 keV. The sputtering rate of $\approx 0.3$ nm/cycle has been significantly smaller than the effective photoelectron escape depth of $\approx 2$ nm [20]. Fig. 5 shows typical interfacial depth profiles of Ga and As 3d core levels of a) \textit{in situ} and b) \textit{ex situ} fabricated Ga$_2$O$_3$-GaAs structures. The 3d binding energies of Ga\textsubscript{GaAs} and As\textsubscript{GaAs} are identical to standard XPS lines reported earlier (19.2 and 41.2 eV, respectively) [21]. The binding energy of Ga\textsubscript{Ga$_2$O$_3$} is 21.2 and 20.8 eV for \textit{in situ} and \textit{ex situ} fabricated interfaces, respectively. The Ga 3d peak gradually shifts from the bulk Ga$_2$O$_3$ to the bulk GaAs on a length scale consistent with the electron escape depth. The intermediate peak can easily be fitted as a sum of two components. Chemical reaction products, in particular As$_2$O$_3$ (44.6 eV) and As$_2$O$_5$ (45.7 eV) are not detectable at both \textit{in situ} and \textit{ex situ} fabricated Ga$_2$O$_3$-GaAs interfaces. Consequently, the chemical reaction $\text{As}_2\text{O}_3 + 2 \text{GaAs} \rightarrow \text{Ga}_2\text{O}_3 + 4\text{As} \ (\Delta G = -62 \text{ kcal/mol})$ [10] resulting in formation of metallic As and degradation of electronic interface properties [11] is excluded. A more detailed discussion of XPS spectra acquired from Ga$_2$O$_3$-GaAs structures is given in [22].

Note that virtually identical, As$_2$O$_y$ and metallic As free, interfacial As 3d core level profiles were obtained from \textit{in situ} fabricated amorphous Al$_2$O$_3$-(100) GaAs and amorphous...
SiO\textsubscript{2}\textsubscript{(100)} GaAs structures as well. However, in sharp contrast to Ga\textsubscript{2}O\textsubscript{3}\textendash GaAs interfaces, these interfaces exhibit a surface recombination velocity \( S \) comparable to that of a bare surface (\( \geq 10^7 \text{cm/s} \)) and a Fermi level pinned at the interface as demonstrated by C-V measurements \([12]\). Evidently, the absence of As\textsubscript{2}O\textsubscript{3} and metallic As is a necessary, but not sufficient, requirement for unpinned interfaces on GaAs. We attribute the fundamentally different electronic interface properties observed at various \textit{in situ} fabricated oxide-GaAs interfaces to the specific atomic structure associated with the interfacial atoms of GaAs and the deposited oxide molecules. Therefore, we have chosen the term \textit{intrinsic} pinning for our observation of Fermi level pinning at \textit{in situ} fabricated SiO\textsubscript{2}\textendash and Al\textsubscript{2}O\textsubscript{3}\textendash GaAs interfaces.

**IV. ELECTRICAL PROPERTIES**

Electrical properties have been investigated by capacitance\textendash voltage (C-V), conductance\textendash voltage (G-V), and current\textendash voltage (I-V) measurements. Quasi-static and high-frequency (100 kHz, 1 MHz) C-V measurements have been performed on MOS capacitors using a Keithley 590 CV Analyzer, a Keithley 595 Quasi-static CV Meter, and a Keithley 230 Programmable Voltage Source. Further C-V characterizations have been carried out at frequencies of 100 Hz, 1 kHz, and 10 kHz using a Hewlett Packard 4284A Precision LCR Meter. All characterizations were done at room temperature in a shielded probe station. Complementary optoelectronic interface characterizations have been performed using the dependence of the photoluminescence intensity \( I_{\text{PL}} \) on the incident light power density on the sample surface.
In this section, we discuss measurement results obtained from in situ fabricated Ga$_2$O$_3$-GaAs structures including C-V, G-V, I-V, and $n$-$P_n$ data. $D_n$ and $S$ will be derived and we will thoroughly investigate the strong inversion regime which has been observed in GaAs for the first time. Figs. 6 and 7 show typical C-V and G-V characteristics, respectively, of (a) n-type and (b) p-type Ga$_2$O$_3$-GaAs MOS structures measured in quasi-static mode and at various frequencies between 100 Hz and 1 MHz. The measured curves have been acquired using low-intensity light illumination ($I_0 = 9.4 \times 10^{14}$ cm$^{-2}$ s$^{-1}$). Here, $I_0$ is the incident light intensity on the sample surface. Note that the optical transmissivity $T$ of our metal dots is $\geq 10^{-4}$ resulting in a significantly lower light intensity $I_0$ entering GaAs. As will be discussed later, low-intensity light illumination is the only viable approach to observe inversion in C-V measurements on epitaxial GaAs due to the small thermal generation/recombination rate of GaAs. We have carefully investigated further effects of low-intensity light illumination, in particular possible implications for the derivation of $D_n$. In Fig. 6, the classical operational modes of ideal MOS structures are clearly revealed and we will discuss the regimes of 1) strong inversion, 2) accumulation, and 3) depletion in the following section. The relative dielectric constant of Ga$_2$O$_3$ films obtained by fitting simulation results to the measurement data is 14.2.

1) Strong Inversion: We have investigated different mechanisms of inversion carrier generation/recombination including thermal generation/recombination and low-intensity light generation. Thermal generation/recombination of minority (inversion) carriers is dominated by bulk trap levels $E_T$ near midgap located within the depletion layer where the Fermi level $E_F$ crosses $E_T$ (crossover point [27]). In our structures, the crossover point is located in the lightly doped epitaxial layers which typically exhibit bulk minority carrier lifetimes $\tau_n$ in excess of 100 ns [23]. The minority carrier response time $\tau_n$ for thermal generation/recombination is given by [27]

$$\tau_n = \frac{1}{\sqrt{2}} \left( \frac{N}{n_i} \right) \tau$$

where $\tau = \sqrt{\tau_p \tau_n}$. With $\tau_p \tau_n = \tau > 100$ ns, $n_i = 2.7 \times 10^6$ cm$^{-3}$, and $N$ in the low $10^{18}$ cm$^{-3}$ range, (2) gives $\tau_n \geq 400$ s. Consequently, we did not observe inversion due to thermal generation/recombination in our C-V measurements even at very low sweep rates. Instead, the samples operate in the deep depletion regime with identical high-frequency and quasi-static capacitance [25].

In contrast to thermal generation/recombination, high generation rates can be readily achieved with low-intensity light illumination. Using our standard microscope illumination and objectives with magnification 2, 10, and 20, optical generation rates for electrons and holes $G_n = G_p \equiv G_0 (\lambda_0 \leq 870$ nm) ranging from $4.6 \times 10^{13}$ to $2.6 \times 10^{15}$ cm$^{-2}$ s$^{-1}$ (12.7 $\leq P_0 \leq 715$ $\mu$W/cm$^2$) are obtained. Here, $\lambda_0$ is the wavelength of the incident light. Note that a light pulse is also often used for C-V measurements on state-of-the-art SiO$_2$-Si ($n_i = 1.4 \times 10^{10}$ cm$^{-3}$) with Si bulk lifetimes of the order of milliseconds in...
order to generate minority carriers when the structure is biased in inversion. In our experiments, leakage currents of up to 200 pA [28] corresponding to \(6 \times 10^{11}\) carriers/cm\(^2\) s required steady state low-intensity light illumination to maintain strong inversion.

We have further evaluated the measured conductance \(G\) in strong inversion (Fig. 7). \(G\) is related to the inversion carrier generation/recombination conductance \(G_{gr}\) by [27]

\[
G = G_{gr} \frac{1}{\left(\omega C_{ox}\right)^2 + \omega^2 (C_{ox} + C_D)^2} \tag{3}
\]

where \(\omega\), \(C_{ox}\), and \(C_D\) are the angular frequency, the oxide capacitance, and the depletion layer capacitance, respectively. In Fig. 7, \(G\) is described by (3) for frequencies \(f \leq 10\) kHz. Series resistance loss, which will be discussed later in conjunction with the accumulation regime, significantly increases for \(f > 10\) kHz and dominates at high frequencies. \(G_{gr}\) is a central component of the MOS equivalent circuit in strong inversion and can be derived from \(G\) or from the measured capacitance \(C\) in strong inversion [27]. For example, Fig. 8(a) shows the conductance \(G\) as a function of frequency with \(I_0\) as a parameter for a Ga\(_2\)O\(_3\)/p-type GaAs structure in strong inversion. \(G_{gr}\) is inferred from the plateaus in the measurement curves using (3) and \(G_{gr}\) is plotted as a function of \(I_0\) in Fig. 8(b). Linear \(G_{gr}-I_0\) relations have been obtained with a regression coefficient of \(6.7 \times 10^{-16}\) and \(8.3 \times 10^{-18}\) S for p- and n-type structures, respectively. Identical values of \(G_{gr}\) have been inferred using the frequency \(\omega_m\) which marks the transition from low-frequency to high-frequency behavior in the measured C-V characteristics [27]. Fig. 8(b) also shows the minority carrier response time \(\tau_R = G_{gr}/C_D\). No attempt has been made to theoretically derive an expression for \(G_{gr}\) as a function of \(I_0\). Note that \(G_{gr}\) does not only depend on the light intensity \(I_0\) entering the semiconductor through the metal dot but is also influenced by minority carriers generated within a diffusion length of the metal dot edge.

The capacitance overshoot at the onset of inversion (Fig. 6) has been consistently observed on both n- and p-type samples and may be attributed to filling of trapping centers in the oxide [28].

2) Accumulation: The frequency dispersion observed in accumulation is caused by oxide layers of relatively low resistivity adjacent to the interface. This reduces the effective oxide thickness and increases the observed capacitance with decreasing measurement frequency (Maxwell–Wagner effect [29]). It also causes an additional component in the G-V measurements which can be described as a series resistance \(R_s\) loss [27]. The Maxwell–Wagner effect can be approximated by an equivalent circuit comprising multiple RC circuits connected in series. The equivalent circuit parameters have been inferred from C-V and G-V measurements in accumulation. For the C-V and G-V results shown in Figs. 6 and 7, respectively, the nonuniformity extends over a depth of \(\approx 10\) nm from the interface and may be related to the depth profile of the Gd concentration (see Section III). The incorporation of Gd gives also rise to trapping effects and charge injection into the oxide which cause long term drift of the capacitance and of device parameters in accumulation [28].

Another interesting feature disclosed in Fig. 6(a) is the quasi-static capacitance being typically smaller in accumulation than in inversion. This is attributed to the low effective density of states in the GaAs conduction band compared to that of the valence band. This characteristic feature has been experimentally observed for the first time and confirmed by calculations based on our selfconsistent device model for semiconductor heterostructures.

3) Depletion: We have inferred \(D_{it}\) using results of C-V and G-V measurements in depletion. Fig. 9 shows typical results obtained for \(D_{it}\) as a function of bandgap energy. We will first discuss \(D_{it}\) obtained from C-V measurements using the quasi-static/high-frequency technique [27]. \(D_{it}\) indicated
by open circles and triangles has been derived from p- and n-type samples, respectively. The inferred midgap interface state density \( D_{it} \) is in the low \( 10^{10} \) \( \text{cm}^{-2} \text{eV}^{-1} \) range. Note that the quasi-static/high-frequency technique requires conclusive evidence that interface traps do not respond to the high-frequency signal. This has been clearly demonstrated in Fig. 6 which shows virtually identical measurement results in depletion above measurement frequencies of 1 kHz.

Further, we have thoroughly studied the effect of low-intensity light illumination and its implications for the derivation of \( D_{it} \). The application of low-intensity light illumination during the measurement causes the electron quasi-Fermi level \( E_{Fn} \) to depart from the hole quasi-Fermi level \( E_{Fl} \) in the semiconductor and modifies the quasi-static and high-frequency C-V curves. This is demonstrated in Fig. 10 for a \( \text{Ga}_2\text{O}_3/n \)-type GaAs structure. Two consequences of illumination on the derivation of \( D_{it} \) have been revealed. Since \( E_{Fn} \neq E_{Fl} \), (1) weak inversion already occurs for \( E_{Fn} > E_i \) (n-type, see Fig. 10) or \( E_{Fl} < E_i \) (p-type), and (2) the occupancy of all interface states located at \( E_i \), between \( E_{Fn} \) and \( E_{Fl} \) is changed when \( (E_{Fn} + E_{Fl})/2 \) crosses the midgap level \( E_i \). Whereas the first implication only restricts the validity range of the quasi-static/high-frequency technique to \( E_i \approx 0.17 \) eV (n-type) and \( E_i \approx 0.17 \) eV (p-type) in our experiments, the second effect can lead to an artificially high result for \( D_{it} \). With respect to the latter finding, the inferred midgap \( D_{it} \) should be considered as an upper limit. More details on the effects of low-intensity light illumination on C-V characteristics will be reported in [25].

For G-V analysis, our measurement results need to be corrected for \( R_s \) [27]. Fig. 11 shows the \( R_s \) corrected high-frequency G-V curves for a \( \text{Ga}_2\text{O}_3/n \)-type GaAs structure. Note that the corrected curves shown in Fig. 11 were not obtained from the G-V results shown in Fig. 7 since interface trap loss is entirely masked by oxide loss (\( R_s \)) for the latter G-V curves. Using the corrected G-V curves, \( D_{it} \) is obtained using

\[
D_{it} \approx \frac{Aq^2 f_{Dw} \left( C_{ox} - C_p \right) / C_{ox}}{2}
\]

where \( A, f_{Dw}, C_p, C_{ox}, \) and \( q \) are the sample area, a universal function \( f_{Dw} \approx 0.12 - 0.4 \), the measured conductance and capacitance at the conductance peak [27], and the electronic charge. Using (4), \( D_{it} = (1.2 \pm 0.7) \times 10^{11} \) and \( (1.5 \pm 0.8) \times 10^{11} \) \( \text{cm}^{-2} \text{eV}^{-1} \) have been obtained in the vicinity of the conduction band edge for \( E = E_c - 0.29 \) eV and \( E = E_c - 0.17 \) eV, respectively (filled triangles in Fig. 9). The relatively large error range for \( D_{it} \) stems from the
approach, but is completely invisible in high-frequency G- V measurements. The time constants of charge trapping of Dit is about an order of magnitude higher when injection levels are > 1 s [28] and depend only indirectly on the position of EF at the semiconductor surface via the carrier concentrations in the semiconductor bands [30].

The interface state density Dit is directly related to the interface recombination velocity S (1). Therefore, we performed complementary studies of the internal quantum efficiency η (derived from P_L) from low injection (ρ < N) to very high injection (ρ > N) over a wide range of incident light power densities \( P_0 \) (1 \( \leq P_0 \leq 10^4 \) W/cm²). Here, \( \rho \) is the injected carrier density. This technique is based on the relative weight of nonradiative \( (R_{SRH}) \) and radiative \( (R_{rad}) \) recombination as a function of \( P_0 \) resulting in a unique curve shape of η versus \( P_0 \) for a specific \( S \) (see, e.g., [31], [32]). This is demonstrated in Fig. 12(a) which shows the measured (symbols) and simulated (lines) efficiency η versus \( P_0 \) of \( n \)-type Ga2O3/n-type GaAs structures and, for comparison purposes, η versus \( P_0 \) of a reference Al0.45Ga0.55As–GaAs interface (n-type). Here, \( P_0 = TP_0 \) where \( T \) is the optical transmissivity of the samples and \( \lambda_0 = 514.5 \) nm is the excitation wavelength. The simulation results have been obtained from calculated PL depth profiles using our self-consistent, numerical interface analysis device model [25], [32]. Note that the analysis has been performed from low to very high injection levels since the calculated carrier densities \( \rho \) are \( 6.5 \times 10^{14} \) and \( 7.8 \times 10^{17} \) cm⁻³ at the semiconductor surface \( (S = 5000 \) cm/s) for the lowest and highest excitation densities \( P_0 \) of 1 and \( 10^4 \) W/cm², respectively. Since the PL intensity is not measured in absolute units, the measured curves are rigidly shifted to the calculated ones [31]. The best fit of the simulations to the measurement data has been attained for \( S = 4000–5000 \) and \( 1000 \) cm/s for Ga2O3– and Al0.45Ga0.55As–GaAs structures, respectively. The above obtained \( S \) at \( n \)-type Ga2O3/n-type GaAs interfaces corresponds to a capture cross section \( \sigma \) of \( \approx 10^{-13} \) cm². Further, Fig. 12(b) shows η versus \( P_0 \) in \( P_L \)-type Ga2O3/p-type GaAs structures. Here, the inferred recombination velocity \( S \) is \( \approx 10^4 \) cm/s. In contrast to the results on \( n \)-type samples, \( \eta \) does not saturate for very high injection levels and exhibits a weaker dependence on \( P_0 \). The observed differences in the \( \eta-P_0 \) characteristics for \( n \)- and \( p \)-type samples are discussed in [25], [32].

**B. Ex Situ Deposited Ga2O3–GaAs Interfaces**

The \( n \)-type device process requires complex equipment and, moreover, it is not applicable to electronic passivation of GaAs surfaces exposed to processing environments during device
 properties to be discussed later. Note that a 36-nm thick SiO2 cap layer has been deposited prior to rapid thermal annealing in order to avoid interface degradation caused by penetrating gas species. This relatively thick SiO2 layer introduces additional surface roughness in the course of sputtering and in turn, decreases the height and increases the spatial extension (not shown) of the acquired Ga2O3-GaAs spectra.

Electronic interface properties of temperature stressed, in situ fabricated Ga2O3-GaAs interfaces have been investigated by standard steady-state PL measurements. Fig. 14 shows typical PL spectra of n- and p-type as-deposited and temperature stressed Ga2O3-GaAs structures as well as of corresponding bare samples. The incident light power density $P_0 = 1060 \text{ W/cm}^2$ and the excitation wavelength $\lambda_0$ are 514.5 nm, respectively. As indicated in Fig. 14, the PL spectra after RTA in forming gas for 30 s at 700 or 800 °C are virtually identical to those obtained from corresponding as-deposited samples. These results imply preservation of excellent electronic interface properties. $I_{PL}$ decreases by only 21% after temperature stress of 1000 °C for 30 s giving a slightly increased recombination velocity $S \approx 8500 \text{ cm/s}$. Note that identical results have been obtained after temperature stress in inert gases such as N2.

B. Photochemical Stability

Fig. 15 shows the relative peak photoluminescence intensity of in situ fabricated n-type Ga2O3-GaAs samples and of an n-type Al0.45Ga0.55As-GaAs reference structure as a function of time $t$ measured for a high-incident light power density $P_0 = 1060 \text{ W/cm}^2$. Here, the unit relative photoluminescence is defined as the PL intensity of the structures under test normalized to the PL of a corresponding bare surface at zero time determined at $P_0 = 1060 \text{ W/cm}^2$. Furthermore, the as-measured PL signals have been corrected for alterations of optical transmissivity $T$. The slope of the measured PL versus time characteristics is $+0.028$, $+0.041$, and $-0.079%/h$ for as-deposited and temperature stressed Ga2O3-GaAs interfaces, and for the Al0.45Ga0.55As-GaAs reference structure, respectively. Thus, in situ fabricated Ga2O3-GaAs interfaces show excellent photochemical stability with no degradation of PL intensity to be observed after 22 h of high-intensity laser excitation. These results imply preservation of excellent interface properties in agreement with the conclusions obtained from the above described temperature stress experiments.

For comparison purposes, an optimized (NH4)2S treatment of a GaAs surface combined with electron cyclotron resonance (ECR) plasma deposition of Si3N4 and subsequent annealing has been performed on n-type bare reference samples. Fig. 15 also shows the best result obtained using the latter technique. In sharp contrast to in situ fabricated Ga2O3-GaAs interfaces, the relative PL intensity of (NH4)2S treated samples decays rapidly from 20 to 2.7 during the first hour of high-intensity light exposure. Note that the relatively low PL of the (NH4)2S treated sample measured at zero time is indicative of $S \approx 10^3 \text{ cm/s}$ for an As-deposited structure.

VI. SUMMARY

The extension of MBE toward deposition of gallium oxide molecules has provided required ingredients for the implementation of thermodynamically stable, low $D_{it}$ oxide-GaAs interfaces for low-power, GaAs-based applications. The following results have been obtained.

1) Excellent electronic interface properties including $D_{it}$ in the low $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and $S = 4000$–6000 cm/s for in situ fabricated Ga2O3-GaAs interfaces, and $D_{it}$ in the upper $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ range and $S = 9000 \text{ cm/s}$ for ex situ fabricated Ga2O3-GaAs interfaces.

2) Strong inversion in both n- and p-type GaAs.

Fig. 14. Typical PL spectra of in situ fabricated n- and p-type as deposited (Ts = 560 °C) and temperature stressed Ga2O3-GaAs structures as well as of corresponding bare samples.

Fig. 15. Measured PL as a function of time normalized to the PL of a corresponding bare surface (at zero time) for in situ fabricated Ga2O3-GaAs interfaces, Al0.45Ga0.55As-GaAs structures, and Si3N4-GaAs samples using (NH4)2S treatment and ECR plasma deposition. All samples comprise identical GaAs epitaxial layers and substrates.
3) Thermodynamic interface stability up to at least 800 °C and photochemical interface stability.
4) Charge trapping in the oxide has been revealed as the dominant trapping mechanism. Alternative Ga2O3 deposition techniques need to be explored to further reduce the total density of trapping centers in the structure and to eliminate the Maxwell–Wagner effect observed in accumulation.

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REFERENCES


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PASSLACK et al.: LOW D. THERMODYNAMICALLY STABLE GaOx \textsuperscript{1+} Ga \textsubscript{x} INTERFACES

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